

- Suppose you are running two processes, P1 and P2, on two different processors, M1 and M2. Each processor has its own data cache. P1 and P2 access six shared variables A, B, C, D, E, and F. Using the Goodman's write-once algorithm, and the table at the top of page 355, show variable access patterns that would generate the following conditions:
 - Read-Miss with a dirty copy.
 - Read-Miss with no dirty copy.
 - Write-Hit to a dirty copy
 - Write-Hit to a reserved copy
 - Write-Hit to a valid copy.
 - Write-miss with a dirty copy.
 - Write-miss with no dirty copy.
 - Read-Hit to a dirty copy.
 - Read-Hit to a valid copy.
 - Read-Hit to a reserved copy.
- Find the collision vector and the minimum cycle time for the following pipeline. The pipeline has 7 resources and 8 stages, and the reservation table looks as follows.

X			X				
	X	X					
		X				X	
			X				
			X			X	X
	X				X		
	X			X			

- Suppose you have a very small (but fully associative) cache with only four blocks. You are running a program that accesses the following memory blocks in the following order. Show the contents of the cache after each access. Do this twice, once assuming the use of a FIFO algorithm and once assuming the use of the LRU algorithm.
1,2,3,4,4,3,2,1,5,6,7,1
- Suppose you are performing the following operation on a pipelined vector processor with pipeline chaining. Assuming that the Addition pipeline has 10 stages, and the multiply pipeline has 20 stages, how many clock cycles will be required to complete the operation?
For I = 1 to 64 do
 A[I] = (B[I] + C[I]) * D[I];
EndFor
- Construct a dataflow graph for the following code segment.

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A = B + 1;
C = D + 2;
If A < 5 then
    E = F + C;
Else
    E = D + A;
Endif
    
```

