

**Each Problem is worth 20 points. Complete at least 5 problems. Exam will be graded on a 100-point scale.**

1. You are designing a memory for a new computer system. Available memory modules have a word size of 32 bits, and a cycle time of 50 ns. We have a CPU that is capable of processing 80,000,000 32-bit words per second. How could we use these modules to build a memory capable of keeping up with the machine. (Think about interleaving.)
2. Find the collision vector and the minimum cycle time for the following pipeline. The pipeline has 5 resources and 8 stages, and the reservation table looks as follows.

<b>X</b>				<b>X</b>			
	<b>X</b>		<b>X</b>				
		<b>X</b>		<b>X</b>		<b>X</b>	
			<b>X</b>				
			<b>X</b>		<b>X</b>		<b>X</b>

3. Suppose you are running a program on a computer with an instruction cache, but no data cache. The program consists of a large loop containing 1000 instructions, and the loop is executed 10000 times. 5000 data operands are fetched during the execution of this loop. An access to memory requires 10 cycles, while an access to the cache requires only 1 cycle. Assume that each instruction is one word long, and assume that cache blocks contain only one word. Assuming that the CPU is capable of executing one instruction per cycle, how long would this program take to execute with a 512-word cache? What about with a 1024-word cache?
4. Design a bus for an 8-bit microprocessor. It must be possible to do read and write operations. Use a separate address and data bus, and use equal widths for both. It must be possible to generate interrupts. It must be possible to construct an external cache, and it must be possible to split the external cache into instruction and data cache.
5. You are designing an instruction pipeline for a new CPU. All instructions have three memory-based operands, two input operands, and one output operand. The machine has no programmable registers. Since it is possible for instructions to compete out of sequence it is necessary to detect not only RAW hazards, but WAR, and WAW hazards. Show the comparisons that must be done between two instructions to determine if there is a hazard between them. Indicate which tests detect which type of hazard.
6. Define the following terms.
  - Superpipelining*
  - Superscalar Architecture*
  - Direct-Mapped, Set Associative, and Fully Associative Cache*
  - Memory Interleaving*
  - Bus Arbitration*
  - RISC/CISC*
  - Locality of Reference*